

## List of Publications

### International Journals: (SCI/Scopus/Refereed Journals)

1. Nilesh Anand Srivastava , Anjali Priya , **Ram Awadh Mishra** ,”Interface trap charge-based reliability assessment of high-k dielectric-modulated nanoscaled FD SOI MOSFET for low power digital ICs: Modeling and simulation” Superlattices and Microstructures, Volume 154, Year 2021
2. Raj Kumar and **Ram Awadh Mishra**,” Design and analysis of RNS-based sign detector for moduli set  $\{2^n, 2^n - 1, 2^{n+1}\}$ ”, *Indonesian Journal of Electrical Engineering and Computer Science*, Vol. 22, No. 1, April 2021, pp. 62-70.
3. Nilesh Anand Srivastava , Anjali Priya , **Ram Awadh Mishra** ,“Analog and radio-frequency performance of nanoscale SOI MOSFET for RFIC based communication systems” *Microelectronics Journal*, Volume 98, Year 2020
4. Raj Kumar, Ritesh Kumar Jaiswal, and **Ram Awadh Mishra** , “Perspective and Opportunities of Modulo  $2^n - 1$  Multipliers in Residue Number System: A Review,” *Journal of Circuits, Systems, and Computers*, vol.29, no.11, p. 2030008, Jan.2020.
5. Nilesh Anand Srivastava, and **Ram Awadh Mishra** , “Linearity Distortion Assessment and Small-Signal Behavior of Nano-Scaled SOI MOSFET for Terahertz Applications,” *ECS Journal of Solid State Science and Technology* 8(12) (Dec.2019) N234-N244.
6. Nilesh Anand Srivastava, Anjali Priya, and **Ram Awadh Mishra** , "Design and analysis of nano-scaled SOI MOSFET-based ring oscillator circuit for high density ICs", *Applied Physics A*, vol.125, Issue 8, pp.533, 07/2019, Published By Springer.
7. Anjali Priya, Nilesh Anand Srivastava, and **Ram Awadh Mishra** , "Design and Analysis of Nanoscaled Recessed S/D SOI MOSFET-Based Pseudo-NMOS Inverter for Low-Power Electronics", *Journal of Nanotechnology*, vol.2019, Issue 4935073, pp.1-12, 03/2019, Published By Hindawi.
8. Anjali Priya, Nilesh Anand Srivastava, and **Ram Awadh Mishra** , "Design of High Speed and Low-Power Ring Oscillator Circuit in Recessed Source/Drain SOI Technology", *ECS Journal of Solid State Science and Technology*, vol.8, Issue 3, pp.N47-N54, 01/2019, Published By The Electrochemical Society.
9. Anjali Priya, Nilesh Anand Srivastava, and **Ram Awadh Mishra** , "Perspective of buried oxide thickness variation on triple metal-gate (TMG) recessed-S/D FD-SOI MOSFET", *Advances in Electrical and Electronic Engineering*, vol.16, Issue 3, pp.380-387, 09/2018, Published By AEEE.
10. Ritesh Kumar Jaiswal, Raj Kumar and **Ram Awadh Mishra** , "Area Efficient Memoryless Reverse Converter for New Four Moduli Set  $2^{(n-1)}, 2^n - 1, 2^n + 1, 2^{(2n+1)} - 1$ ", *Journal of*

Circuits, Systems, and Computers, vol.27, Issue 5, pp.75-(1-13), 05/2018, Published By World Scientific Publishing Company.

11. Ritesh Kumar Jaiswal, Chatla Naveen Kumar, **Ram Awadh Mishra**, "Area Efficient Sparse Modulo  $2^n-3$  Adder", Circuits and Systems, vol.7, Issue 1, pp.4024-4035, 10/2016, Published By Scientific Research Publishing
12. Vadthiya Narendar\*, Saurabh Rai, Siddharth Tiwari, **R. A. Mishra**, "A two-dimensional (2D) analytical subthreshold swing and transconductance model of underlap dual-material double-gate (DMDG) MOSFET for analog/RF applications", Superlattices and Microstructures, vol.100, Issue 1, pp.27-289, 04/2016, Published By Elsevier Ltd.
13. Anjali Priya, **Ram Awadh Mishra**, "A two dimensional analytical modeling of surface potential in triple metal gate (TMG) fully-depleted Recessed-Source/Drain (Re-S/D) SOI MOSFET", Superlattices and Microstructures, vol.92, Issue 1, pp.316-329, 04/2016, Published By Elsevier Ltd.
14. Vadthiya Narendar and **R. A. Mishra**, "Analytical Modeling and Simulation of Multigate Finfet devices and the impact of high-k dielectrics on short channel effects (scs)", Superlattices and Microstructures, vol.85, Issue 1, pp.357-369, 09/2015, Published By Elsevier Ltd.
15. Suman Lata Tripathi, Madhuraj Kumar, **R. A. Mishra**, "3-D Channel Potential Model for doped symmetrical ultra-thin quadruple gate-all-around mosfet", Journal of Electron Devices, vol.21, Issue 1, pp.1874-1880, 05/2015, Published By Euro-Mediterranean Institute for Sustainable Development.
16. Shipra Upadhyay, R. K. Nagaria, **R. A. Mishra**, "Performance Improvement of GFCAL Circuit", International Journal of Computer Applications, vol.78, Issue 1, pp.29-37, 09/2013, Published By Foundation of Computer Science NY, USA.
17. Shipra Upadhyay, R. K. Nagaria, **R. A. Mishra**, "Low Power Adiabatic Computing with improved Quasistatic Energy Recovery Logic", VLSI Design, vol.2013, Issue 1, pp.1-9, 08/2013, Published By Hindawi Publishing Corporation NY, USA.
18. Shipra Upadhyay, **R. A. Mishra**, R. K. Nagaria,, "Performance Analysis of Modified QSERL Circuit", International Journal of VLSI design & Communication Systems(VLSICS), vol.4, Issue 1, pp.19-30, 08/2013, Published By AIRCC Publishing Corporation Chennai, Tamil Nadu, India.
19. S. L.Tripathi, **R. A. Mishra**, "Design of 20 nm FinFET structure with round Fin Corners Using Side Surface Slope Variation", Journal of Electron Devices, vol.18, Issue 1, pp.1537-1542, 08/2013, Published By EuroMediterranean Institute for Sustainable Development LibanPost Hazmieh Str. Beirut- Lebanon.
20. S. L. Tripathi, Ramanuj Mishra, **R. A. Mishra**, "Optimization of High Performance Bulk FinFET Structure Independent of Random Dopent Process Variations", Microelectronics and Solid state Electronics, Issue 1, pp.29-38, 07/2013, Published By Scientific & Academic Publishing Co. USA.

21. Shipra Upadhyay, **R. A. Mishra**, and R. K. Nagaria, "DFAL: Diode Free Adiabatic Logic Circuits", *ISRN Electronics, Hindawi, Publishing Corporation*, vol.2013, Issue 1, pp.1-12, 04/2013, Published By Hindawi Publishing Corporation NY, USA.
22. S. L. Tripathi, **R. A. Mishra**, "Performance Improvement of FinFET using Spacer with High-K dielectric", *Journal of Electron Devices*, vol.17, Issue 1, pp.1447-1451, 03/2013, Published By Euro-Mediterranean Institute for Sustainable Development LibanPost Hazmieh Str. Beirut-Lebanon.
23. A. K. Pandey, J. Tiwari, **R. A. Mishra**, R. K. Nagaria and M. Tiwari, "Design of new low leakage power domino XOR circuit", *International Journal of Computer Applications*, vol.65, Issue 1, pp.28-32, 03/2013, Published By Foundation of Computer Science NY, USA.
24. A. K. Pandey, **R. A. Mishra** and R. K. Nagaria,, "Static switching dynamic buffer circuit", *Journal of Engineering, Hindawi*, vol.2013, Issue 1, pp.1-11, 02/2013, Published By Hindawi Publishing Corporation NY, USA.
25. A. K. Pandey, **R. A. Mishra** and R. K. Nagaria,, "Performance analysis of novel domino XNOR gate in sub 45nm CMOS technology", *WSEAS Transactions on Circuits and Systems*, Issue 1, pp.48-57, 02/2013, Published By World Scientific and Engineering Academy and Society.
26. A. K. Pandey, V. Mishra, **R. A. Mishra**, R. K. Nagaria and V.K.Rao, "Design of a trigger pulse operated low power domino buffer circuit", *The Mediterranean Journal of Electronics and Communication*, vol.9, Issue 1, pp.477-484, 01/2013, Published By SoftMotor Ltd.
27. Shipra Upadhyay, **R. A. Mishra**, R. K. Nagaria,, "Triangular Power Supply Based Adiabatic Logic Family", *World Applied Sciences Journal*, vol.24, Issue 1, pp.444-450, 01/2013, Published By IDOSI Publications L.L.C Dubai UAE.
28. A. K. Pandey, **R. A. Mishra** and R. K. Nagaria, "Leakage power analysis of domino XOR gate", *ISRN Electronics, Hindawi*, Issue 1, pp.1-7, 01/2013, Published By Hindawi Publishing Corporation NY, USA.
29. S. L. Tripathi, Ramanuj Mishra, **R. A. Mishra**, "Multi-gate MOSFET Structures with High-K dielectric Material", *Journal of Electron Devices*, vol.16, Issue 1, pp.1388-1394, 12/2012, Published By Euro-Mediterranean Institute for Sustainable Development LibanPost Hazmieh Str. Beirut- Lebanon.
30. S. L. Tripathi, Ramanuj Mishra, V. Narendar, **R. A. Mishra**, "Optimization of Pie-gate Bulk FinFET Structure", *International Journal of Computer Applications*, vol.59, Issue 1, pp.34-39, 12/2012, Published By Foundation of Computer Science NY, USA.
31. A. K. Pandey, V. Mishra, **R. A. Mishra**, R. K. Nagaria and V. K. Rao,, "Conditional precharge dynamic buffer circuit", *International Journal of Computer Applications*, Issue 1, pp.45-52, 12/2012, Published By Foundation of Computer Science NY, USA.
32. Amit Kumar Pandey, **Ram Awadh Mishra** and Rajendra Kumar Nagaria, "Low Power Dynamic Buffer Circuits", *International Journal of VLSI design & Communication Systems(VLSICS)*,

- Issue 1, pp.53-65, 10/2012, Published By AIRCC Publishing Corporation Chennai, Tamil Nadu, India.
33. S. L. Tripathi, Ramanuj mishra, **R. A. Mishra**, "High FIN Width MOSFET Using GAA Structure", International Journal of VLSI design & Communication Systems(VLSICS), Issue 1, pp.111-121, 10/2012, Published By AIRCC Publishing Corporation Chennai, Tamil Nadu, India.
  34. Sanjeev Rai , Govind Krishna Pal , **Ram Awadh Mishra** and Sudarshan Tiwari, "Design and Analysis of A Charge Recycle Based Novel LPHS Adiabatic Logic Circuits For Low Power Application", International Journal of VLSI design & Communication Systems (VLSICS), Issue 1, pp.123-136, 10/2012, Published By AIRCC Publishing Corporation Chennai, Tamil Nadu, India.
  35. Shipra Upadhyay , R. K. Nagaria, **R. A. Mishra**, "Complementary Energy Path Adiabatic Logic Based Full Adder Circuit", International Journal of Electrical, Computer, Energetic, Electronic and Communication Engineering, Issue 1, pp.542-547, 06/2012, Published By WASET-TURKEY.
  36. V.Narendar, Ramanuj Mishra, Sanjeev Rai, Nayana. R and **R. A. Mishra**, "Threshold Voltage Control Schemes in FINFETS", International Journal of VLSI design & Communication Systems(VLSICS), Issue 1, pp.175-191, 04/2012, Published By AIRCC Publishing Corporation Chennai, Tamil Nadu, India.
  37. V Narendar, Wanjul Dattatray R, Sanjeev Rai, **R. A. Mishra**, "Design of High-performance Digital Logic Circuits based on FinFET Technology", International Journal of Computer Applications, 03/2012, Published By Foundation of Computer Science NY, USA.
  38. Preeti Verma, **R. A. Mishra**, "Temperature Dependence of Propagation Delay Characteristics in LECTOR based CMOS Circuit", Special Issue of International Journal of Computer Applications(0975-8887) on Electronics, Information and Communication Engineering-ICEICE, Issue 1, pp.28-30, 12/2011, Published By Foundation of Computer Science NY, USA.
  39. **R. A. Mishra**, C. Bose, S. K. Sanyal, "Simulation and Microcontroller Implementation of an Integrated Modulo ( $2^n \pm 1$ ) Residue Adder", Advances in Modelling and Analysis Mathematics: Computational Mathematics, Issue 1, pp.35 to 46, 02/2007, Published By AMSE France.

**International/National Conferences:** (Published/Accepted)

1. Nilesh Anand Srivastava, Anjali Priya, and **Ram Awadh Mishra**, "Performance evaluation of Hetero-Gate-Dielectric Re-S/D SOI MOSFET for low Power Applications", 6th IEEE Uttar Pradesh Section International Conference on Electrical, Electronics and Computer Engineering (UPCON 2019), AMU Aligarh.
2. Raj Kumar and **Ram Awadh Mishra**, "A Comprehensive Analysis of Sign Detection in Residue Number System", 6th IEEE Uttar Pradesh Section International Conference on Electrical, Electronics and Computer Engineering (UPCON 2019), AMU Aligarh.

3. Raj Kumar, Ritesh Kumar Jaiswal and **Ram Awadh Mishra**, "Efficient Design for High Speed and Low Area Reverse Converter for High Speed and Low Area Reverse Converter for Moduli Set  $\{2^n, 2^{2n-1}, 2^{2n+1}\}$ ", 6th IEEE Uttar Pradesh Section International Conference on Electrical, Electronics and Computer Engineering (UPCON 2019), AMU Aligarh.
4. Anjali Priya, Nilesh Anand Srivastava, and **Ram Awadh Mishra**, "Performance Investigation of Gate- Engineered Recessed-S/D FDSOI MOSFETs for Low Power Analog/RF applications", In 15th IEEE INDICON 2018, Amrita Vishwa Vidyapeetham, Coimbatore, pp.1-6, 12/2018, Published By IEEE.
5. Narendra Prasad, Nilesh Anand Srivastava, Ritesh Kumar Jaiswal, and **Ram Awadh Mishra**, "Linearity Enhancement of CMOS OTA for High Performance Applications", 5th IEEE Uttar Pradesh Section International Conference on Electrical, Electronics and Computer Engineering (UPCON),, MMMUT GORAKHPUR, pp.1-6, 11/2018, Published By IEEE.
6. Anjali Priya, Nilesh Anand Srivastava, and **Ram Awadh Mishra**, "Impact of Doping Concentration on the performance of TMG Re-S/D FDSOI MOSFET", 5th IEEE Uttar Pradesh Section International Conference on Electrical, Electronics and Computer Engineering (UPCON),, MMMUT GORAKHPUR, pp.1-6, 11/2018, Published By IEEE.
7. R. K. Jaiswal, Megha Bagre and **R. A. Mishra**, Performance Evaluation of Digital and RNS based Filter for Fast DSP Processors, International Conference on Emerging Trends in Computing and Communication Technologies (ICETCCT-2017), GEHU, Dehradun, India, 17-18 November 2017.
8. Anjali Priya, Sanjeev Rai and **R. A. Mishra**, Comparative Analysis of Junctionless Bulk and SOI/SON FinFET, 4th International Conference on Power, Control & Embedded Systems (ICPCES-2017), MNNIT Allahabad, India, 9-11 March 2017.
9. Premlata Singh, Ritesh Jaiswal and **R. A. Mishra**, "New Area Efficient Modulo  $2^{n+1}$  Multiplier", Int. conf. on computing, communication and control technology, SRMU Lucknow, pp.11-14, 11/2016, Published By SRMU
10. Lucky Agarwal, Brijesh Kumar Singh, **R. A. Mishra** and Shweta Tripathi, "Short channel effects (SCEs) characterization of underlapped dual-K spacer in dual-metal gate FinFET device", IEEE International Conference on Control, Computing, Communication and Materials (ICCCCM) - 2016, UCER Naini, Allahabad (U.P), pp.1-6, 10/2016, Published By IEEE.
11. Richa Parihar, V. Narendar and **R. A. Mishra**, Comparative Study of Nanoscale FinFET Structures for High-K Gate Dielectrics, International Conference on Devices, Circuits and Communications, (ICDCCom-2014), BIT Mesra, Ranchi, India, 12-13 September 2014.
12. D. Bhanu Chandar, Narendar Vadthiya, Alok Kumar and **R. A. Mishra**, Suppression of Short Channel Effects(SCEs) by Dual Material Gate Vertical Surrounding Gate(DMGVSG) MOSFET: 3-D TCAD Simulation, International Conference on Design and Manufacturing (IConDM-2013), IIITDM Chennai, India, 18-20 July 2013.

13. Shipra Upadhyay, Prashant Shekhar, R. K. Nagaria and **R. A. Mishra**, "MOS Diode based Adiabatic Logic Circuits", IEEE Conference at Delhi Technological University, DELHI, pp.54-55, 02/2013, Published By IEEE Xplorer.
14. S. L. Tripathi, Ramanuj Mishra, V. Narendar, **R. A. Mishra**, "High Performance Bulk FinFET with Bottom Spacer", IEEE International Conference on Electronics, Computing and Communication Technologies (CONECCT), 2013, IISc Bangalore, pp.1-5, 01/2013, Published By IEEE Xplorer.
15. V. Narendar, Sanjeev Rai, S. L. Tripathi and **R. A. Mishra** and A. K. Singh, "Performance Evaluation of Underlap double-gate and double-metal gate FINFET device for nanoscale applications", International Conference on Emerging Trends in Electrical, Electronics and Communication Technologies (ICECIT), Anantpur, Andhra Pradesh, pp.1-5, 12/2012, Published By Elsevier Proceedings.
16. S.L Tripathi, Ramanuj Mishra, **R. A. Mishra**, Characteristic Comparison of connected DG FINFET, TG FINFET and Independent Gate FINFET on 32 nm Technology, 2<sup>nd</sup> International Conference on Power, Control & Embedded Systems (ICPCES-2012), MNNIT Allahabad, India, 17-19, December 2012, pp. 1-7.
17. A. K. Pandey, S. Kaur, **R. A. Mishra** and R. K. Nagaria, "Leakage power reduction for domino circuits in 45 nm CMOS technologies", ICPCES 2012, MNNIT ALLAHABD, pp.1-5, 12/2012, Published By IEEE Xplorer.
18. Shipra Upadhyay, **R. A. Mishra**, R. K. Nagaria, "Comparative Performance of Irreversible Adiabatic Logic Circuits for Low Power VLSI Design", ICIAICT-2012, Gautam Buddha University, Greater Noida., pp.379-386, 03/2012, Published By Computer Society of India and GBU NOida
19. Pushpa Rani, Amit Kumar Pandey, R. K. Nagaria and **R. A. Mishra**, "A Survey on Different Keeper Design Topologies for High Speed Wide AND-OR Domino Circuits", SCES-2012, MNNIT Allahabad., pp.1-4, 03/2012, Published By IEEE Xplorer.
20. A.K.Pandey, **R. A. Mishra**, R. K. Nagaria, "Low Leakage Power in Sub-45 nm with Multiple Threshold Voltages and Multiple Gate –Oxide Thickness footed Domino Logic", international Conference on Current Trends in Technology NUiCONE, Nirma University, Ahmedabad, pp.1-6, 12/2011, Published By IEEE Xplorer.
21. Preeti Verma, **R. A. Mishra**, "Leakage Power and Delay Analysis of LECTOR Based CMOS Circuits", ICCCT2011, Allahabad, pp.260-264, 09/2011, Published By IEEE Xplorer.
22. Ruchi Singh, **R. A. Mishra**, "Design and Simulation of Diminished-One Modulo  $(2n + 1)$  Adder using Circular Carry Selection", International Conference of Electrical and Electronics Engineering, Imperial College London, U.K., pp.1515-1518, 07/2011, Published By International Association of Engineers, World Congress on Engineering WCE

23. Preeti Verma, **R. A. Mishra**, Temperature Dependence of Propagation Delay Characteristic in LECTOR based CMOS circuit, Proceeding of International Conference on Electronics, Information and Communication systems Engineering (ICEICSE-2011), M.B.M Engineering College, Faculty of Engineering, JNVU, Jodhpur (Rajasthan) India, 28-30 March, 2011.
24. Shivshankar Mishra, V. Narendar, **R. A. Mishra**, On the Design of High-Performance CMOS 1-Bit Full Adder Circuits, International Conference on VLSI, Communication & Instrumentation (ICVCI-2011), SAINTGITS College of Engineering, Kottayam, India, 7-9 April 2011.
25. **R. A. Mishra**, C. Bose, S. K. Sanyal and R. Nandi, "Simulation and Microcontroller Implementation of Residue Multiplier", GSPX-The Embedded Signal Processing Conference, Santa Clara Convention Center, California, pp.19-22, 09/2004, Published By Business Wire.
26. **R. A. Mishra**, C. Bose, S. K. Sanyal and R. Nandi, "Simulation and Microcontroller Implementation of Residue Adder", EDS-04, Czech Republic, pp.25-28, 09/2004, Published By Brno University of Technology.
27. **R. A. Mishra**, C. Bose, S. K. Sanyal and R. Nandi, "A Novel Microcontroller Based Binary To Residue Converter", CODIS 2004, Kolkata, pp.186-189, 01/2004, Published By Jadavpur University.
28. **R. A. Mishra**, C. Bose, S. K. Sanyal and R. Nandi, "A Novel Binary to Residue Converter: Simulation and Hardware Realization", CODEC-04, University of Calcutta, pp.12-15, 01/2004, Published By University of Calcutta.

### **National Conference**

1. **R. A. Mishra**, C. Bose, S. K. Sanyal and R. Nandi, "Simulation and Hardware Realization of Modulo ( $2^n \pm 1$ ) RNS Adder", ACT'05, Durg (Chhattisgarh), pp.365-369, 04/2005, Published By Bhilai Institute of Technology.
2. **R. A. Mishra**, C. Bose, S. K. Sanyal and R. Nandi, "A Microcontroller Based Residue to Binary Converter", NCETEC-2005, Chennai, pp.216-222, 03/2005, Published By Bharath Institute of Higher Education and Research.
3. **R. A. Mishra**, C. Bose, S. K. Sanyal and R. Nandi, "Simulation and Microcontroller Implementation of RNS Based Adder for DSP Applications", INCURSI-2003, New Delhi, pp.25, 11/2003, Published By National Physical Laboratory.

### **Book Chapter**

1. Nilesh Anand Srivastava, Anjali Priya , **Ram Awadh Mishra** , "Analog and Radio-Frequency Performance of Hetero-Gate-Dielectric FD SOI MOSFET in Re-S/D Technology" Lecture Notes in Electrical Engineering, Volume 683, Year 2021, Pages 537-548.
2. Kavindra Kumar Kavi , **R. A. Mishra** , Shweta Tripathi , "Performance Analysis of MoS<sub>2</sub>FET for Electronic and Spintronic Application" Lecture Notes in Electrical Engineering, Volume 683, Year 2021, Pages 489-495.

3. G. Manikanta , **R. A. Mishra** , N. A. Srivastava , R. K. Jaiswal “Design and Analysis of Self-biased OTA for Low-Power Applications” Lecture Notes in Electrical Engineering, Volume 587, Year 2020, Pages 627-637.